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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

10067

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10053970	01/22/2002	438	48	2812	LONG TR: 20

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**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
GERMANY 101 02 432.0 01/19/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed	<input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met	<input type="checkbox"/> yes <input type="checkbox"/> no	MUH-12050
Verified and Acknowledged Examiners's initials		

TITLE : Test circuit for an analog measurement of bit line signals of ferroelectric memory cells
U.S. DEPT. OF COMM. / PAT. & TM. PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	Total Claims Print Claim for O.G.
ISSUE FEE		Primary Examiner	DRAWING
Amount Due	Date Paid		Sheets Drwg. Figs. Drwg. Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE Application Examiner	
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